Abstract of the Disclosure

A method for forming the lower electrode of a capacitor used for fabricating a 1-Gbit or above DRAM, using a material having a high dielectric constant, is used in a method for manufacturing a storage capacitor of a VLSI semiconductor device. The lower electrode, which is to be in contact with a high dielectric film, is formed to have a triple-structured storage node pattern. The lowest layer of the lower electrode is formed with TiN which serves as a barrier against the diffusion of impurities from a lower substrate. The middle layer of the lower electrode is formed with RuO_2 which is easy to pattern. The uppermost layer of the lower electrode is formed with Pt which has excellent leakage current properties.